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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

CHEN, JACK S J

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PA

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	09/900,986		SUBRAMANIAN ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Jack Chen		2813	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4,9-13,15-17 and 19-23 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,9-13,15-17 and 19-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

### **DETAILED ACTION**

In response to the communication filed on October 21, 2004, claims 1-4, 9-13, 15-17 and 19-23 are active in this application.

#### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 21, the phrase "the dielectric layer" lacks antecedent basis.

Re claim 22, the phrase "the dielectric layer" lacks antecedent basis.

Re claim 23, the phrase "the dielectric layer" lacks antecedent basis.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 11-13, 15-17 and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu, U.S./5,688,704.

Re claim 1, Liu discloses a method for forming an IC, which comprises providing a gate dielectric layer 29 (fig. 5) above a top surface of a substrate 11; providing a silicon and nitrogen containing layer 17 (i.e., silicon nitride layer) above the gate dielectric layer (fig. 5); providing an oxide layer 19 above the silicon and nitrogen containing layer (fig. 2); selectively etching the oxide layer to form a first trench in the oxide layer (fig. 4); selectively etching the silicon and nitrogen containing layer to form a second trench (fig. 3) in the silicon and nitrogen containing layer, the second trench being narrower than the first trench and being disposed below the first trench (fig. 4); and providing a gate conductor material 31 in the first trench and the second trench to form the T-shaped gate conductor (fig. 5), see figs. 1-7 and cols. 1-4 for more details.

Re claim 11, Liu discloses a method for forming an IC, which comprises providing a first layer 17 above a substrate 11 (fig. 2), the first layer containing silicon and nitrogen (i.e., silicon nitride); providing an oxide layer 19 over the first layer (fig. 2); selectively etching a first trench in the oxide layer by etching (fig. 4); selectively etching a second trench by etching in the first layer (fig. 3), the second trench having a smaller width than the first trench (fig. 4); and providing a gate conductor material 31 in the first trench and in the second trench to form the T-shaped gate conductor (fig. 5), see figs. 1-7 and cols. 1-4 for more details.

Re claim 15, Liu discloses a method for forming an IC, which comprises providing a first layer 17 above a gate dielectric layer 29 (fig. 5), the gate dielectric layer being above a substrate 11 (fig. 5), the first layer including silicon and nitrogen (i.e., silicon nitride); providing a second layer 19 above the first layer (fig. 2); selectively etching a first aperture in the second layer by etching (fig. 4); selectively etching a second aperture in the first layer utilizing an etching process (fig. 3), wherein the second aperture is narrower than the first aperture (fig. 4); filling the

Art Unit: 2813

first aperture and the second aperture with a gate conductor material 31 (fig. 5); and removing the gate conductor material above the second layer, thereby leaving the T-shaped gate conductor in the first and second aperture (fig. 5), see figs. 1-7 and cols. 1-4 for more details.

Re claims 2 and 12, further comprises removing the oxide layer (figs. 5-6).

Re claims 3 and 13, further comprises removing portions of the silicon and nitrogen containing layer, whereby a pair of spacers 33 remain underneath the gate conductor material in the first trench (fig. 7).

Re claim 17, wherein the gate conductor material is doped or undoped polysilicon material (fig. 5, col. 2, line 63).

Re claim 19, wherein the gate conductor material is silicided (col. 3, lines 20-30).

Re claims 21-23, due to 112 problems, as best can be understood by the examiner is as following: the dielectric layer 19 (fig. 2) is silicon dioxide (col. 2, lines 35-40).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

Art Unit: 2813

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu, U.S./5,688,704.

Liu disclosed above, however, Liu does not explicitly show the width for the first and second trenches as shown in the instant claims 9-10 and using polishing process as shown in claim 4.

It is well known in the art to use polishing process or etch-back process for planarization since both of them provide the same results. Therefore, it is obvious to one having ordinary skill in the art at the time the invention was made to either one of them.

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Liu by selecting the suitable width for the first and second trenches, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

### *Response to Arguments*

8. Applicant's arguments filed March 3, 2004 have been fully considered but they are not persuasive.

Applicant stated that the instant claims 1 and 15 recites that the silicon and nitrogen containing layer is provided above the gate dielectric layer is noted. The prior art also shows this

Art Unit: 2813

feature (i.e., fig. 5, the silicon nitride layer 17 is provided above the gate dielectric layer 29).

Note: this layer (silicon and nitrogen containing layer) does not require to be in direct contact with the gate dielectric layer as shown in the claims. Furthermore, the claims fail to claim the sequential steps for forming the device (i.e., the term “comprising” indicates that the claim is open-ended and allows for additional steps).

Applicant argues that the prior art requires an additional step not required by the instant invention. However, it is noted that the term “comprising” is used (open-end).

Applicant requests the examiner to provide a reference for the instant claim 4 is noted. For example, Lur et al., U.S./5,981,383 teaches using polishing process or etch-back process for planarization, see col. 7, line 9-22.

### *Conclusion*

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2813

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen  
Primary Examiner  
Art Unit 2813

January 5, 2005